IN THE CLAIMS

24. (Added) A method of forming a semiconductor device, comprising:

depositing a dielectric layer over a semiconductor substrate;

patterning and etching a trench opening within the dielectric layer;

depositing a copper layer over the dielectric layer and within the trench opening;

removing portions of the copper layer not contained within the trench opening to define an uppermost copper bond pad;

forming a passivation layer over the uppermost copper bond pad;

patterning and etching the passivation layer to define openings and support structures overlying the uppermost copper bond pad;

depositing a conductive layer over the support structures and within the openings, wherein the conductive layer electrically contacts the uppermost copper bond pad;

patterning and etching the conductive layer to define a capping film over the support structures and the openings.

25. (Added) The method of claim 24, further comprising dielectric studs disposed within the uppermost copper bond pad, wherein at least a part of a support structure overlies a dielectric stud.

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26. (Added) The method of claim 24, wherein the passivation layer includes a material selected from a group consisting of nitrogen-containing silicon oxide, a hydrogen containing silicon oxide, and a carbon containing silicon oxide.

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27. (Added) The method of claim 24, wherein at least one of the support structures is interconnected with unremoved portions of the passivation layer.

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